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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/020,871 | 12/19/2001 | Hyung Sung Jung | HI-0051 | 8800 |

34610 7590 01/10/2007
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| EXAMINER | |
|---|---|
| LEE, ANDREW CHUNG CHEUNG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2616 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 01/10/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/020,871 | JUNG, HYUNG SUNG | |
| | Examiner | Art Unit | |
| | Andrew C. Lee | 2616 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3 and 5-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 1 and 9 are objected to because of the following informalities:

Regarding claim 1, (lines 6 – 7), the term "a even" should be grammatically corrected as "an even", and the term "a odd" should also be grammatically corrected as "an odd".

Regarding claim 9, (lines 5 – 6), the term "a even" should be grammatically corrected as "an even", and the term "a odd" should also be grammatically corrected as "an odd".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 3, 5 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sih et al. (U.S. 6480529 B1), Krasner et al. (US 6724807 B1) and in further view of Van Heeswyk et al. (US 6333926 B1).

Regarding claim 1, Sih et al. disclose the limitation of an apparatus for searching a pilot signal that is received through multiple paths in a CDMA mobile communication system (recited "the ability to search multiple offsets of single pilot" as searching a pilot

signal that is received through multiple paths in a CDMA mobile communication system; Fig. 6, column 3, lines 43 – 53), the apparatus comprising: a coherent accumulator (recited "coherent accumulator" as a coherent accumulator; Fig. 5, elements 430, 432) that accumulates the first and the second despreading signals (Fig, 5, elements 430, 432; column 5, lines 37 – 53); energy calculation means for yielding an energy value using accumulated signals from the coherent accumulator (recited "the coherent accumulations of the I and Q data are completed, the resultant values are squared and summed (I^2 + Q^2) as shown in energy calculator" as energy calculation means for yielding an energy value using accumulated signals from the coherent accumulator; Fig. 5, element 440, column 7, lines 1 – 5); and a non-coherent accumulator that determines an average value of the energy value for a prescribed time (recited "the results of non-coherent accumulator are delivered to DSP where the values are examined to determine which offset in the search window" as a non-coherent accumulator that determines an average value of the energy value for a prescribed time; Fig 5, element 450, column 7, lines 4 – 22). Sih et al. also teach a shift register bank that sequentially stores PN codes (recited "the PN sequences are generated via linear feedback shift register (LFSR) based PN generators" as a shift register bank that sequentially stores PN codes; column 6, lines 22 – 29); a shift register bank that sequentially stores input signals (recited "I and Q data enters shift registers, respectively. Data is continually loaded and shifted through the shift registers at a constant rate" as shift register bank that sequentially stores input signals; Fig. 2, elements 400, 402; column 4, lines 58 – 63; column 12, claim 9, lines 2 – 7); despreading means for despreading the input signals using the PN codes, wherein the

despreading means despreads the input signals in parallel to output despreading signals (Fig. 2, element 410; column 5, 1 – 16). However, Sih et al. do not disclose explicitly a first shift register bank that sequentially stores PN; a second shift register bank that sequentially stores input signals; at least one despreading means for despreading the input signals using the PN codes inputted from the first shift register bank, wherein the despreading means despreads the input signals in parallel to output despreading signals. Krasner et al. disclose the limitation of a first shift register bank that sequentially stores PN (recited "PN sequence is shifted into a PN code coefficient shift register" as first shift register bank that sequentially stores PN; Fig. 2A, "element 14 PN code coefficient shift register" as a first shift register bank); a second shift register bank (that sequentially stores input signals (Fig. 2, elements 400, 402; column 4, lines 58 – 63; column 12, claim 9, lines 2 – 7); a despreading means for despreading the input signals using the PN codes inputted from the first shift register bank, wherein the despreading means despreads the input signals in parallel to output despreading signals (Fig. 2A, element 11 as despreading means and output ("a set of 1023 logicval values 0 and 1" as output) from element 14 PN code coefficient register" as despreading the input signals using the PN codes inputted from the first shift register bank (column 5, lines 8 – 24, lines 29 – 59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sih et al. to include a first shift register bank that sequentially stores PN; a second shift register bank that sequentially stores input signals; a despreading means for despreading the input signals using the PN codes inputted from the first shift register bank, wherein the despreading means despreads the input signals in parallel to output

despreading signals such as that taught by Krasner et al. in order to provide methods and apparatuses for acquiring and tracking Global Positioning System signals or other types of satellite position system signals with a satellite positioning system receiver which includes a matched filter (as suggested by Krasner et al., see column 2, lines 24 – 28).

Sih et al. and Krasner et al. do not disclose explicitly wherein the input signals of an even path are sampled in a first half PN chip and the input signals of an odd path are sampled in a following half chip; first despreading means for despreading the input signals of the even path using the PN codes inputted from the first shift register bank, where the first despreading means despreading means despreads the input signals of the even path in parallel to output first despreading signals; second despreading means for despreading the input signals of the odd path using the PN codes inputted from the first shift register bank, wherein the second despreading means despreads the input signals of the odd path in parallel to output second dispreading signals.

Van Heeswyk et al. disclose the limitation of wherein the input signals of an even path are sampled in a first half PN chip and the input signals of an odd path are sampled in a following half chip (recited "an odd/even splitter 250 takes every even symbol received from the encoder/interleaver and sends it along a first path, and takes every odd symbol received and sends it along a second path" as the input signals of an even path are sampled in a first half PN chip and the input signals of an odd path are sampled in a following half chip; Fig. 5C, column 11, lines 7 – 10); first despreading means for despreading the input signals of the even path using the PN codes inputted from the first shift register bank (recited "the PN spreading block 262 includes PNi and PNq spreading

elements 270,272 on the first path" as first despreading means; Fig. 5C, column 11, lines 15 – 18), where the first dispreading means despreading means despreads the input signals of the even path in parallel to output first despreading signals (Fig. 5C, column 11, lines 15 – 18, lines 20 – 29); second dispreading means for dispreading the input signals of the odd path using the PN codes inputted from the first shift register bank (recited "PNi and PNq spreading elements 274,276 on the second path" as second dispreading means; Fig. 5C, column 11, lines 19 – 20), wherein the second dispreading means despreads the input signals of the odd path in parallel to output second dispreading signals (Fig. 5C, column 11, lines 19 – 20, lines 20 – 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sih et al. and Krasner et al. to include wherein the input signals of an even path are sampled in a first half PN chip and the input signals of an odd path are sampled in a following half chip; first despreading means for despreading the input signals of the even path using the PN codes inputted from the first shift register bank, where the first despreading means despreading means despreads the input signals of the even path in parallel to output first despreading signals; second despreading means for despreading the input signals of the odd path using the PN codes inputted from the first shift register bank, wherein the second despreading means despreads the input signals of the odd path in parallel to output second dispreading signals such as that taught by Van Heeswyk et al. in order to provide a configurable modulator comprising: a first modulator path containing BPSK modulation functions and functions for a first half of a QPSK modulator; a second

modulator path containing functions for a second half of a QPSK modulator as suggested by Heeswyk et al. (see column 1, lines 61 – 65).

Regarding claim 2, Sih et al. disclose the limitation of the apparatus of claimed comprising sorting means for sorting more than one average value of the energy value that are output whenever the input signals are sequentially shifted (column 9, lines 19 – 23).

Regarding claim 3, Sih et al. disclose the limitation of the apparatus of claimed wherein the PN codes and the input signals are stored as a separate I component and Q component, respectively (recited "the PN sequences are generated via linear feedback shift register (LFSR) based PN generator" as PN codes (column 6, lines 22 – 29), "I and Q data enters shift registers, respectively" as input signals are stored as a separate I component and Q component; Fig. 2, elements I, Q, PNI and PNQ; 400, 402; column 4, lines 58 – 63; column 5, lines 1 – 3).

Regarding claim 5, Sih et al. disclose the limitation of the apparatus of claimed wherein the first despreading means (Fig. 6C, element 804A QPSK Despreader as first despreading means) and the second despreading means (Fig. 6C, element 804B QPSK Despreader as second despreading means) each comprise a plurality of despreading device means that are equal in number to each of the PN codes and the input signals (Fig. 6C, column 5, lines 1 – 16; column 9, lines 24 – 39).

Regarding claim 6, Sih et al. disclose the limitation of the apparatus of claimed wherein the plurality of despreading device means (Fig. 6C, elements 804A,

804B,..804H) each are coupled to receive one of the PN codes and one of the input signals, respectively (column 5, lines 1 – 6; column 9, lines 24 – 39).

Regarding claim 7, Sih et al. disclose the limitation of the apparatus of claimed wherein the coherent accumulator comprises a plurality of first adders for accumulating the despreading signals (Fig. 5, elements 421A, 423A); and a plurality of second adders for adding a first accumulation signal and a second accumulation signal, wherein the first accumulation is a signal determined by a first partial coherent accumulation for the PN codes and is stored, and wherein the second accumulation signal is determined by the partial coherent accumulation for next PN codes whenever corresponding next input signals are inputted (Fig. 5, elements 421B, 423B; column 8, lines 10 – 29).

Regarding claim 8, Sih et al. disclose the limitation of the apparatus of claimed wherein the second shift register bank shifts the stored input signals one at a time (Fig. 5, elements 401A, 403A etc. as second shift register bank) and outputs signals corresponding to PN offsets (column 5, lines 1 – 16; column 10, lines 56 – 62).

Regarding claim 9, Sih et al. disclose the limitation of a method for searching a pilot signal received using multiple paths in a CDMA mobile communication system (recited "the ability to search multiple offsets of single pilot" as searching a pilot signal that is received through multiple paths in a CDMA mobile communication system; Fig. 6, column 3, lines 43 – 53), the method comprising: storing PN codes sequentially (recited "the PN sequences are generated via linear feedback shift register (LFSR) based PN generators" as a shift register bank that sequentially stores PN codes; column 6, lines 22 – 29); storing a set of input signals sequentially from a first input signal to a last input

signal (recited "receiving a first type of data and operating as a multiple shift registers when receiving a second type of data, for receiving sets of incoming in-phase first or second type of data" as storing a set of input signals sequentially from a first input signal to a last input signal; column 10; lines 51 – 62; column 12, lines 22 - 26); despreading the set of input signals in parallel by using the PN codes (recited "receiving said set of I data, said sets of Q data, and said PN sequences for producing sets of despread I values and producing sets of despread Q values" as despreading the set of input signals in parallel by using the PN codes); outputting an accumulation signal by accumulating despreaded signals (column 10, lines 64 – 65; column 11, lines 1 – 17; column 12, lines 27 – 31); yielding an energy value of the accumulation signal and an average energy value of the energy value, wherein the average energy value is determined over a prescribed time (column 11, lines 18 – 30; column 12, lines 32 - 37); and determining average mean values corresponding to PN offsets after shifting the set of input signals and repeating the despreading to yielding steps (column 11, lines 31 – 33; column 12, lines 38 – 51). Sih et al. and Krasner et al. do not disclose explicitly wherein the input signals of a even path are sampled in a first half PN chip and the input signals of a odd path are sampled in a following half PN chip; despreading the set of input signals of the even path in parallel by using the PN codes; despreading the set of input signals of the odd path in parallel by using the PN codes; outputting an accumulation signals by accumulating despreading signals of the even path and the despreaded signals of the odd path; Heeswyk et al. disclose the limitation of wherein the input signals of a even path are sampled in a first half PN chip and the input signals of a odd path are sampled in a

following half PN chip (recited "an odd/even splitter 250 takes every even symbol received from the encoder/interleaver and sends it along a first path, and takes every odd symbol received and sends it along a second path" as the input signals of an even path are sampled in a first half PN chip and the input signals of an odd path are sampled in a following half chip; Fig. 5C, column 11, lines 7 – 10 ); despreading the set of input signals of the even path in parallel by using the PN codes (recited "the PN spreading block 262 includes PNi and PNq spreading elements 270,272 on the first path" as despreading the set of input signals of the even path; Fig. 5C, column 11, lines 15 – 18); despreading the set of input signals of the odd path in parallel by using the PN codes (recited "PNi and PNq spreading elements 274,276 on the second path" as despreading the set of input signals of the odd path; Fig. 5C, column 11, lines 19 – 20); outputting an accumulation signals by accumulating dispreading signals of the even path and the despreaded signals of the odd path (column 11, lines 20 – 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sih et al. and Krasner et al. to include wherein the input signals of a even path are sampled in a first half PN chip and the input signals of a odd path are sampled in a following half PN chip; despreading the set of input signals of the even path in parallel by using the PN codes; despreading the set of input signals of the odd path in parallel by using the PN codes; outputting an accumulation signals by accumulating dispreading signals of the even path and the despreaded signals of the odd path such as that taught by Van Heeswyk et al. in order to provide a configurable modulator comprising: a first modulator path containing BPSK modulation functions and functions for a first half of a QPSK modulator; a second

modulator path containing functions for a second half of a QPSK modulator as suggested by Heeswyk et al. (see column 1, lines 61 – 65).

Regarding claim 10, Sih et al. disclose the limitation of the method of claimed wherein the shifting shifts the set of input signals by one so that a penultimate input signal becomes the last input signal and an additional input signal becomes the first input signal, further comprising sorting the energy mean values corresponding to the PN offsets (column 6, lines 33 – 51).

Regarding claim 11, Sih et al. disclose the limitation of the method of claimed further comprising: storing in a buffer more than one first accumulation signal determined by partial coherent accumulation yielded where the input signals are shifted sequentially when a length of coherent accumulation is a multiple of a size of the coherent accumulation unit; and adding a corresponding more than one stored first accumulation signal and a corresponding more than one second accumulation signal yielded whenever a new partial coherent accumulation results are yielded (column 11, lines 1 – 23).

Regarding claim 12, Sih et al. disclose the limitation of the method of claimed wherein the addition is performed corresponding to an order of storing said more than one first accumulation signals in the buffer and an order of yielding said more than one second accumulation signals (recited " an I accumulator for receiving said complete I sums and accumulating them in sets to produce a set of accumulated I sums" as performed corresponding to an order of storing said more than one first accumulation signals in the buffer, and recited " an Q accumulator for receiving said complete Q sums and accumulating them in sets to produce a set of accumulated Q sums" as an order of

yielding said more than one second accumulation signals; column 11, lines 1 – 30).

Regarding claim 13, Sih et al. disclose the limitation of the method of claimed wherein the despreading is executed after a prescribed number of the PN codes and the input signals are stored (column 12, claim 11, lines 20 – 37).

Regarding claim 14, Sih et al. disclose the limitation of the method of claimed wherein a number of the despreading signals is determined by the coherent accumulation unit length (recited "each sum is an N-chip coherent accumulation of a particular offset" as number of the despreading signals is determined by the coherent accumulation unit length; column 5, lines 37 – 40, lines 51 – 61).

### *Response to Arguments*

4. Applicant's arguments filed on 11/02/2006 with respect to claims 1 – 3, 5 – 14 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Khaleghi et al. (US 6618430 B1) teach systems and methods for receiving signals modulated with a carrier frequency, wherein the signals include spreading chip sequences having at least one zero. The invention includes a method of receiving and despreading spread spectrum signals wherein the

spread spectrum signals include spreading chip sequences having at least one zero and at least one non-zero chip.

- Clark (US 6873664 B1) discloses receiver that receives a long pseudonoise (PN) code signal composed of two shorter codes interleaved with one another, includes a correlator unit that correlates the received signal with one or more reference codes corresponding to the two interleaved codes, respectively, and generates correlation signals.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-

3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ACL/ Jan 04, 2006

WING CHAN
SUPERVISORY PATENT EXAMINER